FORM PTO-1449 Application Number Docket Number (Optional) 162.7106USU 10/896,071 Applicant INFORMATI SURE CITATION IN AN APPLICATION Bhattacharya et al. Filing Date Group Art Unit (Use several sheets if necessary) 2811 June 29, 200 U. S. PATENT DOCUMENTS FILING DATE IF **EXAMINER DOCUMENT** DATE NAME **CLASS SUBCLASS APPROPRIATE** -INITIAL NUMBER FOREIGN PATENT DOCUMENTS Translation **CLASS SUBCLASS** YES DOCUMENT DATE COUNTRY NO NUMBER OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.) Kazuo Taki, "A Survey for Pass-Transistor Logic Technologies", IEEE, 1998. Mineo Kaneko and Jialin Tian, "Concurrent Cell Generation and Mapping for CMOS Logic Circuits", IEEE, 1997. C. P. Liu and J. A. Abraham, "Transistor Level synthesis for Static CMOS Combinational Circuits", Proc. 9th Great Lake Symposium on VLSI, pp. 172-175, 1999. DATE CONSIDERED **EXAMINER** Umando

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